

REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claim 40 stands rejected under 35 U.S.C. §112, first paragraph, for allegedly failing to describe the subject matter of the present invention in such a way to enable one skilled in the art to which it pertains to make and/or use the invention. Claims 23, 25-27 and 36-40 stand rejected as allegedly unpatentable over U.S. Patent No. 5,710,450 to Chau, et al. ("Chau, et al.") in view of U.S. Patent No. 5,830,775 to Maa, et al. ("Maa, et al."). Claim 28 stands rejected, under 35 U.S.C. §103(a), as allegedly unpatentable over Chau, et al. in view of U.S. Patent No. 5,510,295 to Cabral Jr., et al. ("Cabral Jr., et al.").

Referring to the §112 rejection of Claim 40, it is the Examiner's position that the applicants fail to disclose the structural features of an electrical contact, where the electrical contact has a SiGe layer, which does not substantially extend beyond the edges of a metal disilicide. Applicants respectfully disagree and submit the following.

The test of enablement is whether one reasonably skilled in the art could make or use the invention with information known in the art without undue experimentation. *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988). First, it is known within the art that metal silicide regions are electrical contact regions for semiconducting devices. Second, FIGS. 1(a)-(f) illustrate a method of making the inventive silicide structure. Third, the originally filed specification describes how a SiGe interlayer is formed at that interface between the silicide and the Si substrate in a manner which would enable one of ordinary skill in the art to make the inventive electrical contact. The applicants' arguments are now discussed in greater detail.

Applicants note that refractory silicides are well known within the semiconductor art as electrical contacts. “Refractory metal silicides are important in wafer fabrication because of the need to reduce the electrical resistance of the many silicon contacts in the source/drain and gate region for chip performance.” Michael Quirk, *Semiconductor Manufacturing Technology*, Prentice Hall Inc., pg. 309 (2001)(ISBN 0-13-081520-9). The specification need not disclose what is well known to those skilled in the art and already available to the public. *In re Buchner*, 929 F.2d 660, 661; 18 USPQ2d 1331, 1332 (Fed. Cir. 1991). Additionally, referring to Page 14 paragraph 3 of the originally filed specification, the applicants have defined the structure of the inventive electrical contact to include a substrate 10 of a silicon-containing material and a first layer of a metal disilicide 24, where the substrate 10 and the metal disilicide are separated by a SiGe interlayer 22, as depicted in FIG. 1F and recited in Claim 40. The applicant may define in the claims what they regard as their invention, essentially in whatever terms they choose, so long as the terms are not used in ways that are contrary to the accepted meaning in the art. *See In re Swinehart*, 439 F.2d 210, 160, USPQ 226 (CCPA 1971). Therefore, since it is known within the art that silicides are electrical contacts and since the claimed electrical contact is described in a manner consistent with the meaning of the art the applicants have provided an electrical contact for the purposes of 35 U.S.C. §112, paragraph 1.

Applicants further submit that FIGS. 1(a) – 1(f) depict a silicide structure, known within the art as an electrical contact, and is not merely an order of layers in cross-section, as alleged by the Examiner. Applicants disclose, referring to Page 7 paragraph 2, that FIGS. 1(a)-1(f) illustrate the basic processing steps of the present invention, which utilizes a metal Ge alloy as the silicide starting material. As discussed above, it is well known within the art that silicides function as the electrical contacts to semiconducting materials.

Applicants further disclose how the SiGe interlayer is formed at the interface between the silicide and the Si substrate in a manner, which would enable one of ordinary skill in the art to make the inventive contact. Referring to Page 11 paragraph 2, applicants disclose where a structure is annealed so as to form a metal silicide layer and a Si-Ge interlayer; where the interlayer separates the silicide from the substrate. Applicants further disclose, “that during this annealing step of the present invention the Ge diffuses to the interface formed between the substrate and the metal alloy layer.” Additionally, FIG. 1C depicts where the SiGe interlayer 22 is formed between the metal silicide layer 20 and the substrate 10.

Finally, applicants disclose annealing parameters that would produce the inventive SiGe layer having lateral edges, which do not substantially extend beyond the metal disilicide. Referring to Page 12 paragraph 2, applicants disclose that, “to form the silicide layer and the Si-Ge interlayer in the structure, annealing is carried out using a rapid thermal anneal process using a gas atmosphere, e.g., He, Ar, Ne or forming gas, at a temperature of about 400°C to about 700°C for a time period of about 300 seconds or less using a continuous heating regime or a ramp and soak heating regime.” The disclosed annealing temperature range provides enough thermal energy to produce the SiGe interlayer by diffusing Ge to the interface between the metal silicide and the substrate; but does not provide enough energy to diffuse the Ge into the Si substrate. Applicants note that the interface between the metal silicide and the substrate is known in the art to include both a vertical (sidewall interface) and a horizontal (base interface) dimension. Applicants have enabled one of ordinary skill in the art to produce the inventive SiGe layer having edges not extending past the overlying metal disilicide, because the disclosed annealing temperatures do not cause the Ge to diffuse beyond the interface of the metal disilicide and the Si substrate in both the horizontal and vertical direction.

Based on the above remarks, the §112 rejection has been obviated; therefore reconsideration and withdrawal of the instant rejection to Claim 40 is respectfully requested.

Applicants further submit that the applied prior art fails to teach or suggest an electrical contact including a first layer of metal disilicide having lateral edges, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a *Si-Ge interlayer having lateral edges which do not substantially extend beyond the lateral edges of the metal disilicide*, as recited in Claim 40.

Chau, et al., referring to FIGS. 3C to 3D, disclose depositing a SiGe semiconducting layer 314 atop a substrate; forming spacers 318 atop the SiGe semiconducting layer 314; and then forming silicide regions 320 atop the SiGe semiconducting layer 314 and adjacent the spacers 318, where the lateral edges of the SiGe semiconducting layer 314 further extend beyond the silicide region 320. Therefore, Chau, et al. fail to teach or suggest an electrical contact structure including a *Si-Ge interlayer having lateral edges, which do not substantially extend beyond the lateral edges of the metal disilicide*, as recited in claim 40.

Additionally, applicants submit that one of ordinary skill in the art could not modify Chau, et al. in a manner to produce the applicants' claimed structure, since Chau, et al. teach away from forming a *Si-Ge interlayer having lateral edges, which do not substantially extend beyond the lateral edges of the metal disilicide*. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Chau, et al. disclose, referring to Column 6 lines 35-40, where a solid-state diffusion step occurs directly after the formation of semiconductor material 314 with a rapid thermal process

(RTP) at a temperature between 800°C to 1000°C for 5 to 60 seconds in a nitrogen N₂ ambient. The temperature range disclosed in Chau, et al. is greater than the applicants' annealing temperature range, which includes temperatures of less than about 700°C. Chau, et al. disclose where during the solid-state diffusion step, dopants (Ge) are able to easily diffuse in a single direction (laterally) below the first sidewall spacer 310 and underneath the outside edge of polysilicon gate electrode 306. Chau, et al. further disclose, referring to Column 6 lines 50-58, that the lateral diffusion results in an ultra shallow tip 317, which is characterized by a very sharp and abrupt junction with the substrate 300 and that an abrupt junction improves the punch-through characteristics of the fabricated transistor. Therefore, since Chau, et al. teach that it is advantageous to promote lateral diffusion of Ge, Chau, et al. lead away from the applicants claimed electrical contact having a *Si-Ge interlayer having lateral edges that do not substantially extend beyond the lateral edges of the metal disilicide*, as recited in Claim 40.

Maa, et al. provide a raised source/drain electrode structure including a metal disilicide layer. Maa, et al. do not teach or suggest forming a SiGe interlayer between the metal disilicide and the substrate. Therefore, Maa, et al. fail to teach or suggest the applicants' claimed electrical contact including a *Si-Ge interlayer having lateral edges, which do not substantially extend beyond the lateral edges of the metal disilicide*, as recited in Claim 40.

Cabral Jr., et al. provide a method of forming a silicide where a precursory metal 16 is deposited atop a refractory metal 14 atop a Si substrate 10, where a silicide is formed following anneal process steps. Cabral Jr., et al. do not teach or suggest forming a SiGe interlayer between the metal disilicide and the substrate. Therefore, Cabral Jr., et al. fail to teach or suggest the applicants' claimed electrical contact including a *Si-Ge interlayer having lateral edges, which do not substantially extend beyond the lateral edges of the metal disilicide*, as recited in Claim 40.

Now referring to the §103 rejections of Claims 23, 25-28 and 36-40, applicants respectfully submit that the applied references fail to teach or suggest all of the claimed limitations of the applicants' electrical contact, as recited in amended Claim 23. Applicants have amended Claim 23 to recite an electrical contact having a first layer of metal disilicide which includes an additive or Ge, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, where said Si-Ge interlayer has a Ge concentration of about .01% to about 9.0 atomic percent. Support for this amendment is found on Page 9 paragraph 2 of the specification. Applicants have also added Claim 41, which recites where the SiGe interlayer has a Ge concentration of about 0.01 to about 2.0 atomic percent. Support for newly added Claim 41 is found on Page 15 paragraph 4 of the specification.

Applicants submit that the applied prior art references fail to teach or suggest an electrical contact including a Si-Ge interlayer having a Ge concentration of about 0.01 to about 9.0 atomic percent, as recited in amended Claim 23. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970). Chau, et al. disclose, referring to Column 5 lines 60-63, a SiGe alloy layer 314 with germanium comprising approximately 10-50% of the alloy. Therefore, Chau, et al. fail to teach or suggest a SiGe interlayer having a Ge concentration of about .01 atomic percent to about 9.0 atomic percent, as recited in amended Claim 23. Chau, et al. also fail to teach or suggest a SiGe interlayer having a Ge concentration ranging from about .01 atomic percent to about 2.0 atomic percent, as recited in newly added Claim 41.

The applied secondary references fail to fulfill the deficiencies of Chau, et al. since the applied secondary references also fail to teach or suggest the applicants' claimed electrical contact including a SiGe interlayer having a Ge concentration ranging from about .01 atomic percent to about 9.0 atomic percent. As discussed above the applied secondary references, Maa, et al. and Cabral Jr., et al., fail to teach or suggest an electrical contact having a SiGe interlayer. Therefore, the applied secondary references fail to teach or suggest an electrical contact including a having a *Ge concentration ranging from about .01 atomic percent to about 9.0 atomic percent*, as recited in amended Claim 23. The applied secondary references also fail to teach or suggest an electrical contact having a SiGe interlayer having a Ge concentration ranging from .01 atomic percent to about 2.0 atomic percent, as recited in newly added Claim 41.

Based on the above amendments and remarks, the §103 rejections have been obviated; therefore reconsideration and withdrawal of the instant rejection are respectfully requested.

Wherefore, reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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